Video Article

Experimental Methods for Trapping Ions Using Microfabricated Surface Ion Traps

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Abstract

Ions trapped in a quadrupole Paul trap have been considered one of the strong physical candidates to implement quantum information processing. This is due to their long coherence time and their capability to manipulate and detect individual quantum bits (qubits). In more recent years, microfabricated surface ion traps have received more attention for large-scale integrated qubit platforms. This paper presents a microfabrication methodology for ion traps using micro-electro-mechanical system (MEMS) technology, including the fabrication method for a 14 μm-thick dielectric layer and metal overhang structures atop the dielectric layer. In addition, an experimental procedure for trapping ytterbium (Yb) ions of isotope 174 ($^{174}Yb^{+}$) using 369.5 nm, 399 nm, and 935 nm diode lasers is described. These methodologies and procedures involve many scientific and engineering disciplines, and this paper first presents the detailed experimental procedures. The methods discussed in this paper can easily be extended to the trapping of Yb ions of isotope 171 ($^{171}Yb^{+}$) and to the manipulation of qubits.

Video Link

The video component of this article can be found at https://www.jove.com/video/56060/

Introduction

A Paul trap can confine charged particles, including ions in empty space, using a combination of a static electric field and a varying electric field oscillating at radio frequency (RF), and the quantum states of the ions confined in the trap can be measured and controlled[1,2,3]. Such ion traps were originally developed for precise measurement applications, including optical clocks and mass spectroscopy[4,5,6]. In recent years, these ion traps have also been actively explored as a physical platform to implement the quantum information processing attributed to the desirable characteristics of trapped ions, such as long coherence times, ideal isolation in an ultra-high vacuum (UHV) environment, and the feasibility of individual qubit manipulation[7,8,9,10]. Since Kielpinski *et al.*[11] proposed a scalable ion-trap architecture that can be used to develop quantum computers, various types of surface traps, including junction traps[12,13], multi-zone trap chips[14], and 2-d array traps[15,16,17], have been developed using semiconductor process-derived microfabrication methods[18,19,20,21]. Large-scale quantum information processing systems based on the surface traps have also been discussed[22,23,24].

This paper presents experimental methods for trapping ions using microfabricated surface ion traps. More specifically, a procedure for fabricating surface ion traps and a detailed procedure for trapping ions using the fabricated traps are described. In addition, detailed descriptions of various practical techniques for setting up the experimental system and trapping ions are provided in the **Supplementary Document**.

The methodology for microfabricating a surface ion trap is given in step 1. **Figure 1** shows a simplified schematic of a surface ion trap. The electric fields generated by the voltage applied to the electrodes in the transverse plane are also shown[25]. An RF voltage is applied to the pair of RF electrodes, while all other electrodes are kept at RF ground; the ponderomotive potential[26] generated by the RF voltage confines the ions to the radial direction. The direct current (DC) voltage applied to the multiple DC electrodes outside the RF electrodes confine the ions to the longitudinal direction. The inner rails between the RF electrodes are designed to help tilt the principal axes of the total potential in the transverse plane. The methodology for designing a DC voltage set is included in the **Supplementary Document**. In addition, more details for designing the essential geometric parameters of surface ion-trap chips can be found in[27,28,29,30,31].

The fabrication method introduced in step 1 was designed considering the following aspects. First, the dielectric layer between the electrode layer and the ground layer should be sufficiently thick to prevent electrical breakdown between the layers. Generally, the thickness should be over 10μm. During the deposition of the thick dielectric layer, the residual stress from the deposited films can cause bowing of the substrate or damages to the deposited films. Thus, controlling the residual stress is one of the key techniques in the fabrication of the surface ion traps. Second, the exposure of the dielectric surfaces to the ion position should be minimized because stray charges can be induced on the dielectric material by scattered ultraviolet (UV) lasers, which in turn results in a random shift of ion position. The exposed area can be reduced by designing overhang electrode structures. It has been reported that surface ion traps with electrode overhangs are resistant to charging under

typical experimental conditions[32]. Third, all the materials, including various deposited films, should be able to withstand 200 °C baking for approximately 2 weeks, and the amount of outgassing from all materials should be compatible with UHV environments. The design of the surface ion-trap chips microfabricated in this paper is based on the trap design from[33], which was successfully used in various experiments[32,33,34,35]. Note that this design includes a slot in the middle of the chip for loading neutral atoms, which are later photo-ionized for trapping.

After the fabrication of the ion-trap chip, the chip is mounted and electrically connected to the chip carrier using gold bonding wires. The chip carrier is then installed in a UHV chamber. A detailed procedure for preparing a trap chip package and the design of the UHV chamber are provided in the **Supplementary Document**.

Preparation of the optical and electrical equipment, as well as the experimental procedures for trapping ions, are explained in detail in step 2. The ions trapped by the ponderomotive potential are generally subject to the fluctuation of the surrounding electric field, which continuously increases the average kinetic energy of the ions. Laser cooling based on Doppler shift can be used to remove the excess energy from the motion of the ions. **Figure 2** shows the simplified energy-level diagrams of a $^{174}Yb^{+}$ ion and a neutral ^{174}Yb atom. Doppler cooling of $^{174}Yb^{+}$ ions requires a 369.5-nm laser and a 935-nm laser, while photo-ionization of neutral ^{174}Yb atoms requires a 399-nm laser. Steps 2.2 and 2.3 describe an efficient method to align these lasers to the surface ion-trap chip and a procedure to find the proper conditions for photo-ionization. After the optical and electrical components are prepared, trapping ions is relatively straightforward. The experimental sequence for trapping ions is presented in step 2.4.

Protocol

1. Fabrication of the Ion-trap Chip Package

1. **Microfabrication of the surface ion-trap chip.**
   NOTE: The process conditions described in this section provide only a rough reference, since the optimal parameters for each process can vary significantly for different equipment. The temperature conditions are given only for the high-temperature processes, such as oxidation and chemical vapor deposition. The fabrication process is carried out using 100 mm-diameter silicon wafers.
   1. Prepare a single crystalline silicon wafer with a thickness of 500-525 µm and clean it using piranha solution for 15 min.
   2. Thermally oxidize the silicon wafer in a furnace tube to form 0.5 µm-thick SiO_2 dielectric layers on both sides.
      NOTE: These layers can electrically isolate the silicon substrate from the ground layer. The process parameters used in the wet-oxidation were: O_2 flow rate of 6,500 sccm, N_2 flow rate of 5,000 sccm, H_2 flow rate of 7,000 sccm, process temperature of 900 °C, and process time of 4.5 h (see the **Table of Materials** for equipment details).
   3. Deposit 0.2 µm-thick Si_3N_4 layers on both sides of the wafer using a low-pressure chemical vapor deposition (LPCVD) process (**Figure 3a**) to protect the thermal oxide layers during the wet-etching process shown in **Figure 3k**.
      NOTE: The process parameters used in the LPCVD process are: H_2SiCl_2 flow rate of 30 sccm, NH_3 flow rate of 100 sccm, pressure of 200 mTorr, and process temperature of 785 °C. This results in a deposition rate of 40 Å/min (see the **Table of Materials** for equipment details).
   4. Deposit a 1.5 µm-thick Al/Cu (1%) layer on the wafer using a sputtering process and the following parameters: Ar flow rate of 40 sccm, pressure of 2 mTorr, and RF power of 300 W.
      NOTE: This results in a deposition rate of 130 Å/min (see the **Table of Materials** for equipment details).
      NOTE: This layer provides a ground plane to prevent RF loss through the silicon substrate and also provides contact points for wire-bonding pads. The aluminum alloy with 1% copper is used to prevent whisker formation during the baking process to achieve a UHV environment. This composition is essential for whisker prevention.
   5. Spin a 2 µm-thick positive photoresist layer on the wafer and lithographically pattern it to define the RF shielding plane and wire-bonding pads.
      NOTE: The process parameters for the 2 µm-thick photoresist are: spin speed of 5,000 rpm, spin time of 40 s, pre-bake temperature of 95 °C, pre-bake time of 90 s, exposure energy of 144 mJ/cm^2, develop time of 60 s, post-bake temperature of 110 °C, and post-bake time of 5 min (see the **Table of Materials** for chemical and equipment details).
   6. Pattern the 1.5 µm-thick Al/Cu (1%) layer using a conventional dry-etching process (reactive ion etching (RIE) or inductive coupled plasma (ICP) etching), with the photoresist patterned in step 1.1.5 as the etching mask.
      NOTE: An ICP etcher should be used with the following process parameters: BCl_3 flow rate of 20 sccm, Cl_2 flow rate of 30 sccm, pressure of 5 mTorr, and RF power of 750 W. This results in an etch rate of 3,600 Å/min (see the **Table of Materials** for equipment details).
   7. Remove the photoresist used in step 1.1.6 usung an O_2 plasma ashing process (**Figure 3b**).
      NOTE: The process parameters for the ashing process are: O_2 flow rate of 150 sccm, pressure of 0.75 mTorr, and RF power of 300 W (see the **Table of Materials** for equipment details).
   8. Deposit a 14 µm-thick SiO_2 layer on both sides of the wafer using plasma-enhanced chemical vapor deposition (PECVD) processes (**Figure 3c**).
      NOTE: The process parameters used in the PECVD process are: SiH_4 flow rate of 540 sccm, pressure of 1.9 Torr, process temperature of 350 °C, and RF power of 750 W. This results in a deposition rate of 3,000 Å/min (see the **Table of Materials** for equipment details). Since depositing the 14 µm-thick SiO_2 layer is one of the most difficult processes, the details are further described in the **Discussion**.
   9. Spin a 6 µm-thick positive photoresist layer on the front of the wafer and lithographically pattern it to define via-holes to electrically connect DC electrodes to the wire-bonding pads.
      NOTE: The process parameters for the 6 µm-thick photoresist are: spin speed of 5,000 rpm, spin time of 40 s, pre-bake temperature of 95 °C, pre-bake time of 5 min, exposure energy of 900 mJ/cm^2, develop time of 10 min, post-bake temperature of 110 °C, and post-bake time of 5 min (see the **Table of Materials** for chemical and equipment details).
   10. Pattern the 14 µm-thick SiO_2 layer on the front of the wafer using a conventional RIE process, with the photoresist patterned in step 1.1.9 as the etching mask.

NOTE: The process parameters for SiO_2 etching are: CHF_3 flow rate of 25 sccm, CF_4 flow rate of 5 sccm, Ar flow rate of 50 sccm, pressure of 130 mTorr, and RF power of 600 W. This results in an etch rate of 3,600 Å/min (see the **Table of Materials** for equipment details).

11. Remove the photoresist used in step 1.1.10 with an O_2 plasma ashing process. Dip the wafer into a heated solvent or sonicate it before ashing (**Figure 3d**).
12. Spin a 6 µm-thick positive photoresist layer on the backside of the wafer and lithographically pattern it to form an oxide hard mask for the deep reactive ion etching (DRIE) of silicon substrate (**Figure 3j**).
13. Pattern the 14 µm-thick SiO_2 layer on the backside of the wafer using a conventional RIE process, with the photoresist patterned in step 1.1.12 as the etching mask.
14. Remove the photoresist used in step 1.1.13 with an O_2 plasma ashing process (**Figure 3e**).
15. Deposit a 1.5 µm-thick Al/Cu (1%) layer, which is used as the electrode using a sputtering process.
16. Deposit a 1 µm-thick SiO_2 layer on the wafer using a PECVD process (**Figure 3f**).
17. Spin a 2 µm-thick positive photoresist layer on the wafer and lithographically pattern it to define the electrodes.
18. Pattern the 1.5 µm-thick Al/Cu (1%) layer and the 1 µm-thick SiO_2 layer using a conventional ICP etching process, with the photoresist patterned in step 1.1.17 as the etching mask.
19. Remove the photoresist used in step 1.1.18 with an O_2 plasma ashing process (**Figure 3g**).
20. Spin a 6 µm-thick positive photoresist layer on the wafer and lithographically pattern it to define the 14 µm-thick oxide pillar patterns.
21. Pattern the 14 µm-thick SiO_2 layer using a conventional RIE process, with the photoresist patterned in step 1.1.20 as the etching mask.
22. Remove the photoresist used in step 1.1.21 with an O_2 plasma ashing process (**Figure 3h**).
23. Spin a 6 µm-thick positive photoresist layer on the wafer and lithographically pattern it to expose the loading slot.
24. Pattern the SiO_2 and Si_3N_4 layers using a conventional RIE process, with the photoresist patterned in step 1.1.23 as the etching mask.
25. Remove the photoresist used in step 1.1.24 with an O_2 plasma ashing process (**Figure 3i**).
26. Pattern the silicon substrate from the backside of the wafer using a DRIE process (**Figure 3j**).
    NOTE: The etch depth should be measured repeatedly to prevent the penetration of the silicon substrate from the backside. The target etch depth is approximately 450-470 µm. The DRIE process was performed with iterations of C_4F_8 deposition for 5 s, C_4F_8 etch for 3 s, and Si etch for 5 s. In the C_4F_8 deposition step, the flow rates of C_4F_8, SF_6, and Ar were 100, 0.5, and 30 sccm, respectively. Note that Ar is used to accelerate the etch rate of C_4F_8 and Si, but it is also applied in the C_4F_8 deposition step, with the same flow rate, to stabilize the pressure condition. In the C_4F_8 etch step, the flow rates were changed to 0.5, 50, and 30 sccm, respectively. In the Si etch step, flow rates of 0.5, 100, and 30 sccm, respectively, were used. The RF power and the chamber pressure were set to 825 W and 23 mTorr in all steps. For these conditions, the etch rate of the Si was 1 µm for each loop (see the **Table of Materials** for equipment details).
27. Dice the wafer into 10-mm x 10-mm pieces using a dicing machine.
28. Detach the dicing tape from the die by dipping it in acetone for 5 min. Clean the die by dipping it in running deionized (DI) water for 10 min and isopropyl alcohol (IPA) for 2 min. Dry it for 2 min at 110 °C.
29. Etch the sidewalls of the oxide pillars to fabricate electrode overhang structures using an oxide wet etching process for 60 s in a buffered oxide etchant (BOE), which is (NH_4F:HF=6:1) (**Figure 3k**). Clean the die by dipping it in running DI water for 10 min and IPA for 2 min. Dry it for 2 min at 110 °C.
30. Penetrate the slit-shaped ion loading hole from the front of the die using a DRIE process.
    NOTE: The fabrication process of the ion-trap chips is complete at this step (**Figure 3l**).

2. Preparation of Optical and Electrical Equipment and Trapping ions

NOTE: The fabricated trap chip is packaged with a chip carrier, and the chip carrier is installed in a UHV chamber. While procedures for fabricating the trap-chip package and for preparing the UHV chamber are provided in the **Supplementary Document**, this section describes the details for setting up optical and electrical equipment and for trapping ions.

1. **Preparation of electrical connections.**
    1. Connect a multi-channel digital-to-analog converter (DAC) to the feedthrough at the backside of the UHV chamber to apply voltage to the corresponding DC control electrodes.
       NOTE: **Figure 4** shows one example of the voltage applied to the trap chip. The detailed method for designing such a DC voltage set is described in the **Supplementary Document**.
    2. Connect a current source to an oven pin in the feedthrough at the back.
    3. Add a directional coupler between an RF generator and the helical resonator. Connect the signal from the RF generator to the output port of the directional coupler. Also, connect the input port of the directional coupler to the input port of the helical resonator.
       NOTE: This configuration allows for monitoring the reflected power from the helical resonator[36].
    4. Adjust the position of the helical resonator cap and scan the frequency of the generator to find the frequency at which the reflection is at a minimum. Repeat this step until the global minimum is found.
       NOTE: The frequency at the global minimum is the resonant frequency. Use of a spectrum analyzer with a tracking generator option or measurement of the S_{11} parameter with a network analyzer can simplify the scanning process for the minimum reflection. If any of the electrical connections with a DAC voltage source or current source for the oven is changed, the impedance of the RF feedthrough is changed, and the resonant frequency will shift.
    5. Turn off the RF generator.
       Caution: When the helical resonator is applying high RF voltage to the trap, do not change any electrical connections that can cause impedance changes. Sudden impedance changes can easily burn the bonding wires of the chip.

2. **Alignment of the 369.5 nm laser and the imaging system.**
    1. Collimate the 369.5-nm laser from an optical fiber using a collimator and try to match the height of the collimator from the surface of the optical table to the height of the chip; make the beam propagate horizontally.

2. Set the propagating direction of the collimated 369.5-nm beam towards the trap chip, through either the left or right viewport of the UHV chamber, as shown in **Figure 5**. Coarsely align it such that the laser beam propagates parallel to the trap-chip surface and almost touches the surface of the chip.
3. Mount a focusing lens for the 369.5-nm laser on a translation stage. Place the focusing lens along the propagating direction so that the laser will be focused in the vicinity of the trapping position above the chip surface and so that the focused laser propagates along the trap-chip surface. Adjust the position of the focusing lens with the translation stage; the position of the laser beam focus will follow the movement of the focusing lens.
4. Place a high-numerical-aperture imaging lens mounted on a translation stage in front of the UHV chamber, considering the distance from the chip surface (**Figure 5**).
5. Align the 369.5-nm beam with the trap-chip surface so that there is some amount of laser scattering from the chip surface.
   NOTE: The scattered light collected by the imaging lens will form a faint image around the image plane of the lens. This image can generally be observed, even with fluorescent paper when the area is sufficiently dark.
6. Adjust the position of the imaging lens until the image on the fluorescent paper becomes sharp.
7. Place an electron-multiplied charged-coupled device (EMCCD) mounted on a translation stage, considering the location of the imaging plane of the lens, found in the previous step.
8. Mount an infrared (IR) filter in front of the EMCCD to block the black body radiation from the oven when the oven is heated for evaporation.
9. Mount a 369.5-nm bandpass filter in front of the EMCCD to block the background light.
10. Compare the image of the EMCCD with the layout of the electrodes. Adjust the positions of the EMCCD and the image lens until the electrodes can be seen with the EMCCD. Align both the imaging lens and the EMCCD until the image becomes sharp.
11. Identify which electrodes are shown in the EMCCD and align the EMCCD to match its center to the expected trapping location.
12. Align the 369.5-nm beam vertically so that it will pass through the trapping position. To find out the distance between the center of the beam and the trap surface, move the beam towards the trap surface until the scattering of the beam is maximized.
    NOTE: After step 2.2.12, it can be assumed that the center of the beam is right on the chip surface.
13. From the numerical simulation of the trap potential[29], find the expected height of the ion trapping position from the chip surface. Move the 369.5 nm beam away from the chip surface by the expected height using the micrometer of the lens translation stage.Move the imaging lens and the EMCCD back by the same distance. Write down the micrometer readings of the imaging lens and the EMCCD.

3. **Alignment of the 399 nm and 935 nm lasers and the oven test.**
   1. Replace the 369.5 nm bandpass filter with a 399 nm bandpass filter. From the numerical simulation of the imaging lens, find the difference between the focal length of 399-nm light and that of 369.5-nm light resulting from the chromatic aberration. Adjust the longitudinal positions of the imaging lens and the EMCCD to make the 399-nm focused on the EMCCD.
   2. Collimate the 399 and 935 nm beams, delivered from the optical fibers, with the respective collimators, and adjust the heights of the fiber collimators to match the height of the chip to make both beams propagate horizontally.
   3. Align the 399 nm beam towards the trap-chip surface through another viewport such that the 399 nm laser is propagating in the opposite direction from the 369.5 nm laser. Try to make the collimated 399 nm laser overlap with the focused 369.5 nm laser.
   4. Combine the collimated 935 nm beam with the collimated 399 nm laser using a dichroic mirror and align the 935 nm beam such that the 935 nm laser co-propagates with the 399-nm laser. To check how well the two beams are overlapping with each other, divert those two beams with a temporary mirror before they enter the chamber and measure the locations of the beams along the beam path using either a beam profiler or a pinhole. If space is insufficient for placing the temporary mirror between the chamber and the focusing lens, consider putting the optical setup on a small optical breadboard; the degree of overlap can be checked at a separate place.
   5. Mount a focusing lens for both lasers on an additional translation stage and set the focusing lens between the dichroic mirror and the temporary mirror. Estimate the distance from the temporary mirror to the trapping position and adjust the location of the focusing lens such that the 399 nm laser is focused at the trapping position (**Figure 6b**).
   6. Check whether the focus of the 399 nm laser coincides with the focus of the 935 nm laser. If the two foci do not overlap, finely align the 935 nm laser.
   7. Remove the temporary mirror in the 399 nm laser path. Check the trace of the 399 nm laser on the chip surface using EMCCD. If no trace of the 399 nm laser beam can be observed, move the 399 nm beam path around the chip. Also, slightly adjust the distance between the chamber and the imaging lens until the image of the chip surface becomes sharp.
   8. Align the trace of the 399 nm beam on the chip surface such that it will pass the expected trapping position. Similar to the 369.5 nm beam alignment, move the 399-nm beam towards the chip surface until the intensity of the scattered light becomes maximized.
   9. Move the 399 nm laser beam away from the chip surface by the same height used in step 2.2.13 using a micrometer. Move the imaging lens and the EMCCD back by the same distance.
   10. Put the temporary mirror used in step 2.3.4 back. Repeat step 2.3.6 and then remove the temporary mirror.
       NOTE: After step 2.3.10, the 935 nm laser can be assumed to be passing through the trapping position above the chip surface.
   11. Set the wavelength of the 399 nm laser close to the $^1S_0$-$^1P_1$ transition of ^{174}Yb (751,526 GHz). Turn on the current for the oven filled with naturally occurring Yb and gradually increase the current.
       NOTE: In general, evaporation does not necessarily start at the same current found by the residual gas analyzer (RGA), as described in the **Supplementary Document**, so try different current values until evaporation is observed. Only when the neutral Yb atoms start to evaporate and the frequency of the laser is resonant with the $^1S_0$-$^1P_1$ transition of one of the Yb isotopes, the neutral Yb atoms will start to absorb the laser light and re-emit it such that the fluorescence from the Yb can be observed with the EMCCD. Generally, the resonant frequencies measured by a wavelength meter are shifted from the nominal values, ranging from tens to hundreds of MHz. Therefore, for each current setting, scanning the laser frequency with a span range of 1 GHz and a step of less than 50 MHz is recommended.
   12. Once the resonant fluorescence from the naturally occurring oven is observed, reduce the current until the fluorescence cannot be observed.
   13. Scan the laser around the first resonant frequency and write down the amount of fluorescence at each resonance. Compare the distribution of the fluorescence strength and the spacing between the resonances with the values from[37]. Identify the resonance frequencies for the different isotopes.

NOTE: The resonance of ^{174}Yb has been measured to be approximately 751.52646(2) THz. However, this value is slightly shifted by the Doppler effect, and the measured value can vary depending on the accuracy of the wavelength meter.

4. **Trapping ions.**
    1. Replace the 399 nm bandpass filter with the 369.5 nm bandpass filter and move the imaging lens and the EMCCD back to the position obtained in step 2.2.13 so that the 369.5-nm fluorescence emitted by trapped ions can be imaged at the EMCCD.Check the alignment of all the lasers one more time by repeating step 2.2.12 and using UV and IR viewing cards for the visual inspection of the beam overlap.
    2. Check that the voltages of the DAC are properly set. Turn on the RF generator at a very low power setting and gradually increase the output power. Also, make sure that the reflected power from the helical resonator is still the minimum by scanning the RF frequency around the resonance.
    Caution: Make sure that the amplified voltage at the trap chip does not exceed the breakdown voltage. In atmospheric pressure, the dielectric strength of an SiO_2 film is known to be approximately 10^7 V/cm, but this value cannot be assumed in the UHV environment. Although the exact breakdown voltage in the UHV environment is not explicitly measured, the 8-μm lateral gap of the trap chip in a 10^{-11}-Torr vacuum withstands 240 V of RF voltage amplitude in the experimental setup.
    3. Set the frequency of the 399-nm laser to the resonance frequency of ^{174}Yb, identified in step 2.3.13. Set the frequency of the 935-nm laser for the $^{174}Yb^+$ isotope.
    NOTE: With a wavelength meter, 320.57199(1) THz can be used, but due to the limited accuracy of wavelength meters, there can be a variation up to tens of MHz.
    4. Set the frequency of the 369.5-nm laser at a value that is ~100-200 MHz less than the resonance frequency so that even if there is some amount of inaccuracy with the wavelength meter, the frequency will be still red-detuned.
    NOTE: Here, 200-MHz detuning is subtracted from the expected resonance when the expected resonant frequency of the $^{174}Yb^+$ is around 811.29152(1) THz.
    5. Turn on the current source for the oven and increase the current slowly until it reaches the value found in step 2.3.12. Wait for a few minutes. If no ion is trapped, increase the current by ~0.1-0.2 A and wait again. If the ion is still not trapped, check whether the reflected RF is still at the minimum and then gradually increase the output power of the RF generator.
    Caution: Make sure that the amplified voltage at the trap chip does not exceed the expected breakdown voltage.
    6. Briefly block the 935 nm laser and check whether there is any change in the image.
    NOTE: If the EMCCD settings (including the electron-multiplying (EM) gain, exposure time, and contrast of the image) are not within a proper range, even when an ion is trapped, it is not easy to tell whether the change of intensity in the vicinity of the trapping region is caused by a real trapped ion or by the change in the scattering of the 369.5 nm laser. Because of the IR filter, the EMCCD camera cannot show any change in the 935 nm laser, so blocking the 935 nm laser does not make any change to the image when there is no trapped ion. However, if an ion is trapped, the scattering rate of the 369.5 nm laser drops significantly without the 935 nm laser. Therefore, the change to the EMCCD image caused by blocking the 935 nm laser is a good indicator of the success of trapping ions.
    Caution: If the 935 nm laser is blocked for too long, the trapped ion gets heated and might escape the trap.
    7. Turn off the oven after the ions are trapped. Try to find the resonance of the 369.5 nm laser by gradually increasing the frequency.
    NOTE: As the frequency gets closer to the resonance, the scattering rate will increase, but once the resonance is crossed, the 369.5 nm laser starts heating the ion rather than cooling it, which in turn causes the image of the trapped ion to become unstable. Once the resonance frequency of the 369.5 nm laser is found, reduce the frequency of the laser by 10 MHz from the resonance.
    8. Scan the frequency of the 935 nm laser until the scattering rate of 369.5 nm gets maximized.
    9. Adjust the locations of the imaging lens and the EMCCD camera until the image of the ion sharpens.

Representative Results

Figure 7 shows the scanning electron micrographs (SEM) of the fabricated ion-trap chip. The RF electrodes, inner DC electrodes, outer DC electrodes, and loading slot were successfully fabricated. The sidewall profile of the dielectric pillar became jagged because the PECVD oxide was deposited in several steps. The multiple deposition steps were used to minimize the effects of residual stress from thick oxide films. This is further described in the **Discussion**.

Figure 8 shows the EMCCD image of five $^{174}Yb^+$ ions trapped using the microfabricated ion-trap chip. The trapped ions can last for more than 24 h with continuous Doppler cooling. The number of trapped ions can be adjusted between 1 and 20 by changing the applied DC voltage set. This experimental setup is very reliable and robust and has currently been in operation for 50 months.

Figure 9 shows the shuttling of trapped ions along the axial direction. The ion position in **Figure 9b** is displaced from that in **Figure 9a** through the adjustment of the position of the DC potential minimum by changing the DC voltages.

Figure 10 shows preliminary results of Rabi oscillation experiments with a $^{171}Yb^+$ ion. To obtain the results, the additional setups described in the **Supplementary Document** were used. The results were included to show a potential application of the experimental setup explained in this paper.

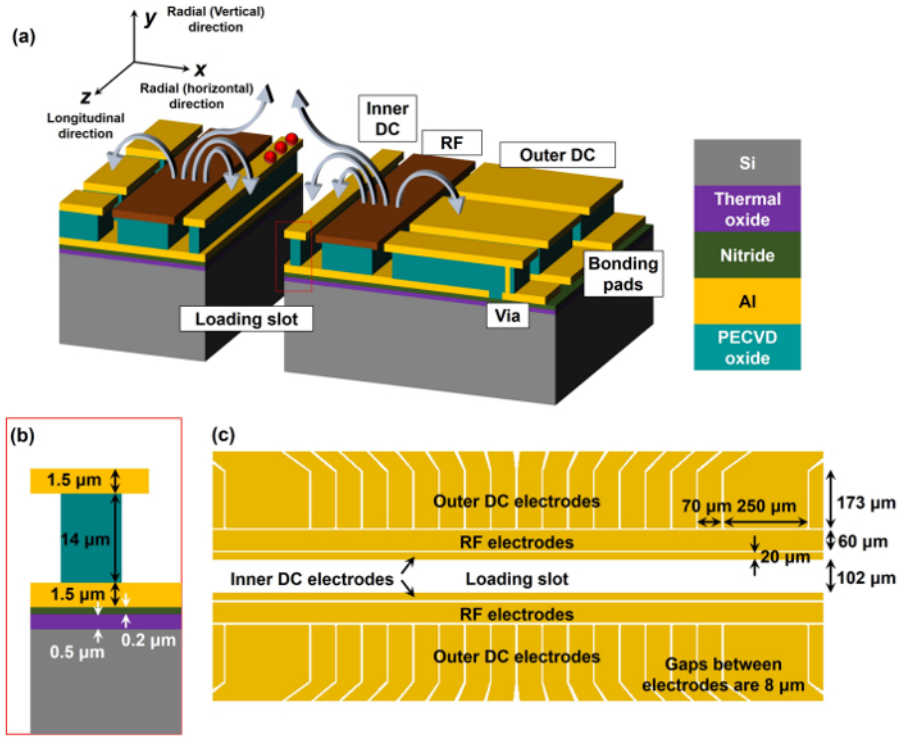

Figure 1: Schematic of the surface ion trap. (**a**) The red dots represent the trapped ions. The brown and yellow electrodes indicate the RF and DC electrodes, respectively. The gray arrows show the direction of the electric field during the positive phase of the RF voltage. Note that the schematic is not drawn to scale. (**b**) The vertical dimensions of the electrode structure. (**c**) The lateral dimensions of the electrode structure. Please click here to view a larger version of this figure.

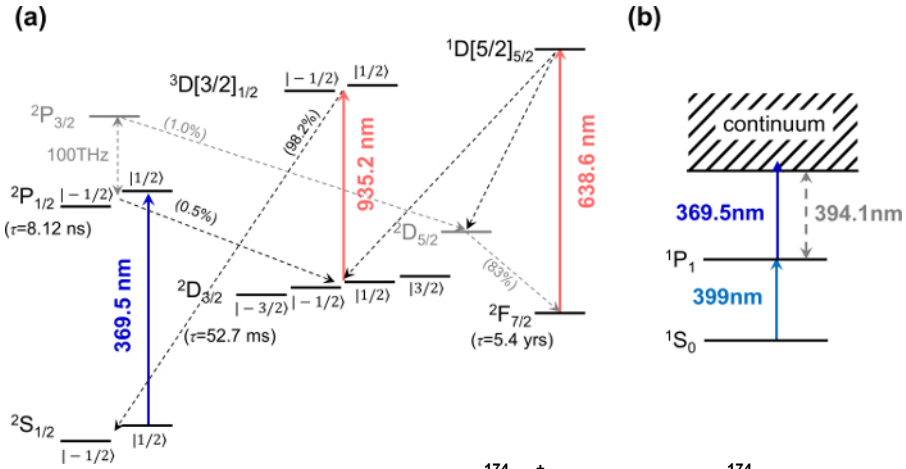

Figure 2: Simplified energy-level diagrams of a $^{174}Yb^+$ ion and a neutral ^{174}Yb atom. (**a**) When a 369.5 nm laser is detuned to the red side (lower frequency) of the resonance, a cycling transition between $^2P_{1/2}$ and $^2S_{1/2}$ reduces the kinetic energy of the ion because of the Doppler effect. Occasionally, a small but finite branching ratio makes the electron decay from $^2P_{1/2}$ to $^2D_{3/2}$, and a 935-nm laser is required to return the electron back to the main cycling transition. The electron can also decay into a $^2F_{7/2}$ state once per hour, on average, and a 638 nm laser can pump it out of the $^2F_{7/2}$ state, but this is not necessary for a simple system[38]. The values in the ket notation represent the projections of the total angular momenta J along the quantization axis m_J. (**b**) To ionize neutral atoms evaporated from the oven, a two-photon absorption process was used[39]. A 399 nm laser excited an electron to $^1P_1$ state, and the 369.5 nm photon for Doppler cooling had more energy than necessary to remove the excited electron from the ion. Please click here to view a larger version of this figure.

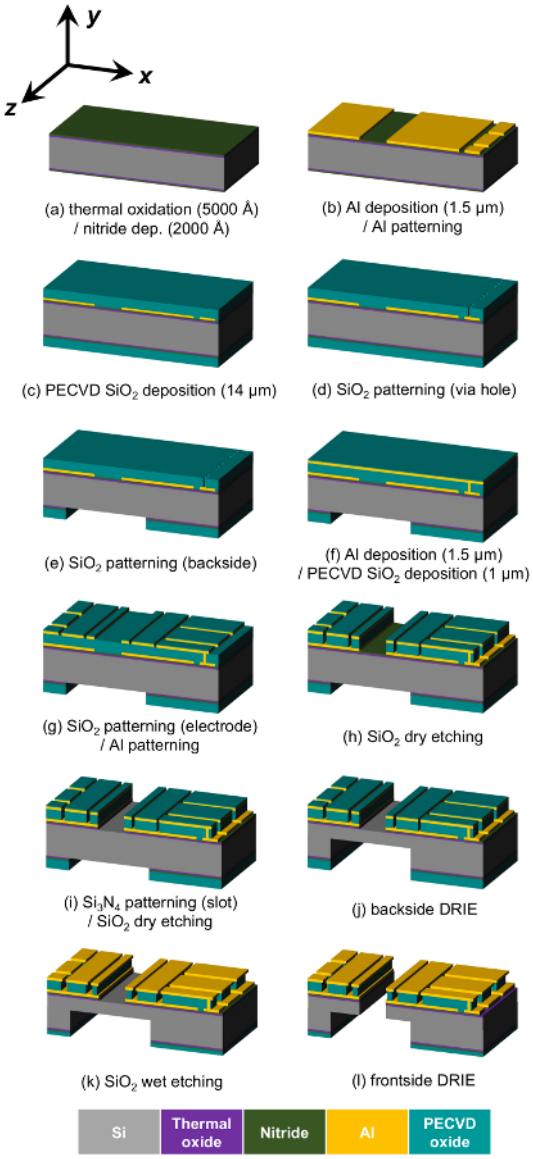

Figure 3: Fabrication process flow of a surface ion trap. (**a**) Thermal oxidation to grow a 5,000 Å-thick SiO_2 layer and LPCVD of a 2,000 Å-thick Si_3N_4 layer. (**b**) Deposition and ICP etching of a 1.5 μm-thick sputtered Al layer. (**c**) Deposition of a 14 μm-thick SiO_2 layer on the both sides of the wafer using PECVD processes. (**d**) Patterning of the 14 μm-thick SiO_2 layer deposited on the front of the wafer using an RIE process (**e**) Patterning of the 14 μm-thick SiO_2 layer deposited on the back of the wafer using an RIE process. (**f**) Deposition of a 1.5 μm-thick sputtered Al layer and a 1 μm-thick PECVD SiO_2 layer. (**g**) Patterning of the 1.5 μm-thick Al layer using an ICP process and the 1 μm-thick SiO_2 layer using an RIE process. (**h**) Patterning of the 14 μm-thick SiO_2 layer deposited on the front of the wafer using an RIE process. (**i**) Patterning of the 5,000 Å-thick SiO_2 layer and the 2,000 Å-thick Si_3N_4 layer using an RIE process. (**j**) DRIE of the silicon substrate 450 μm from the back of the wafer. (k) Wet-etching of the SiO_2 layer on the Al electrodes and the sidewalls of the dielectric pillars. (**l**) Penetration of the silicon substrate from the front through a DRIE process. Note that the schematics are not drawn to scale. Please click here to view a larger version of this figure.

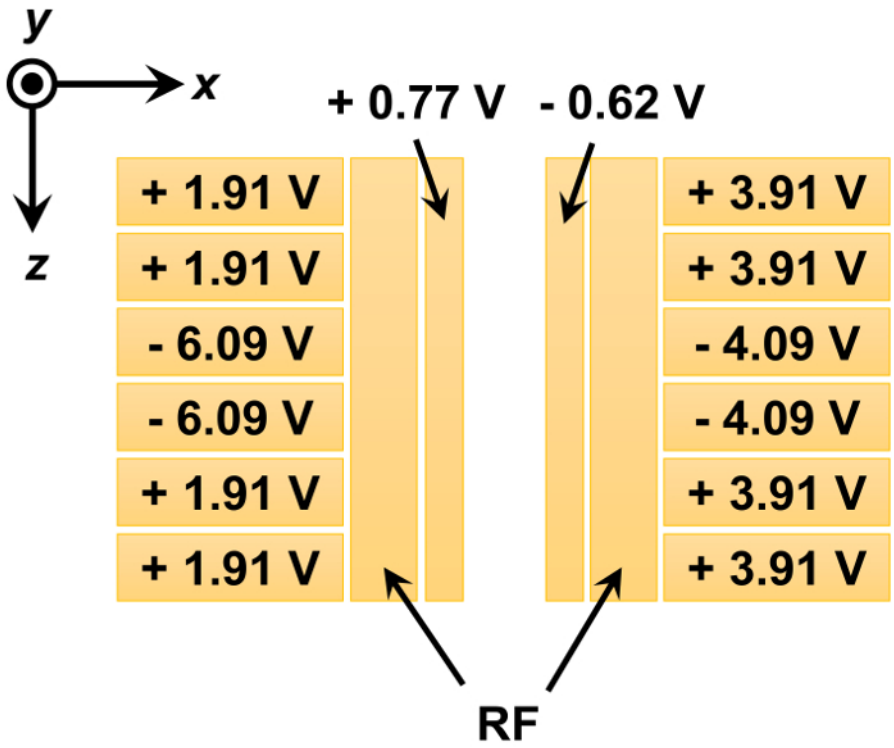

Figure 4: An example of the DC voltage set used to trap ions. The voltages applied to the inner rails can compensate for the asymmetric electric field in the horizontal direction to tilt the principal axes of the total potential in the transverse plane. The axial trap frequency generated by the voltage set was 550 kHz. Please click here to view a larger version of this figure.

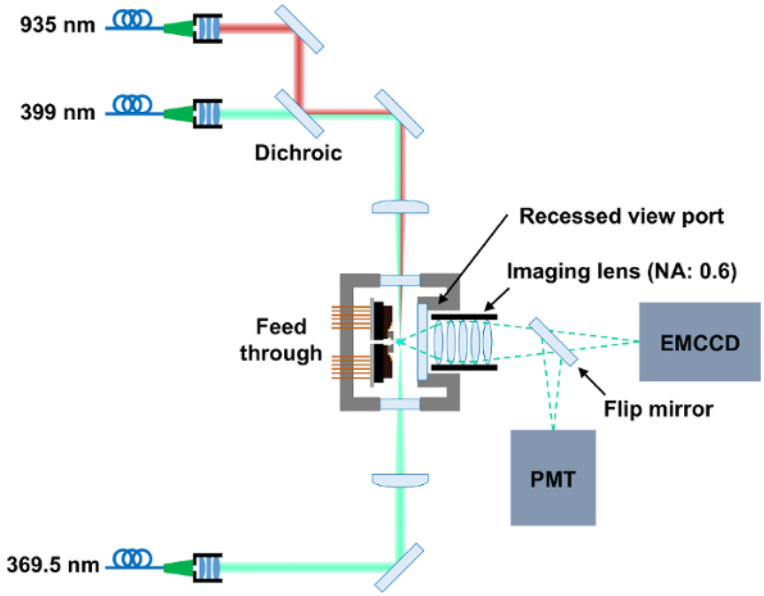

Figure 5: Schematic of the optical setup. Three diode lasers are aligned to overlap at the trapping position. The recessed viewport of the UHV chamber allows the imaging lens to be placed as close as possible to the chip surface. A flip-mirror placed between the imaging lens and the EMCCD allows for the selective monitoring of the ion fluorescence using either a photon multiplied tube (PMT) or an EMCCD. Please click here to view a larger version of this figure.

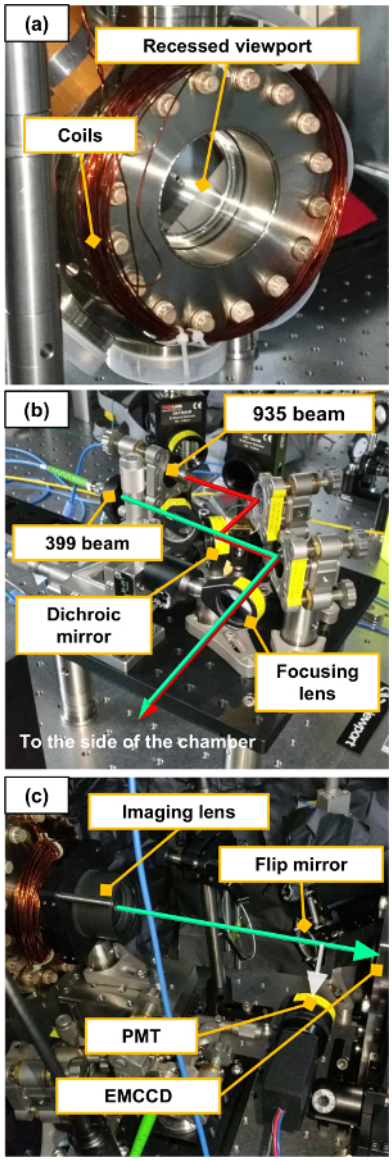

Figure 6: Images of the constructed optical setup. (**a**) A coil is wound around the front viewport of the chamber to generate a magnetic field, which can break degenerate energy levels of ytterbium ions. (**b**) The optical setup for steering the 399 nm and 935 nm beams. The red and green lines indicate the beam path of the 935 nm and 399 nm lasers, respectively. (**c**) The configuration of the imaging system, including the flip-mirror, the imaging lens, the EMCCD, and the PMT. The path of the fluorescence emitted from the trapped ions can be determined by the flip-mirror. The green and white arrows indicate the path of the fluorescence when being monitored by the EMCCD and the PMT, respectively. Please click here to view a larger version of this figure.

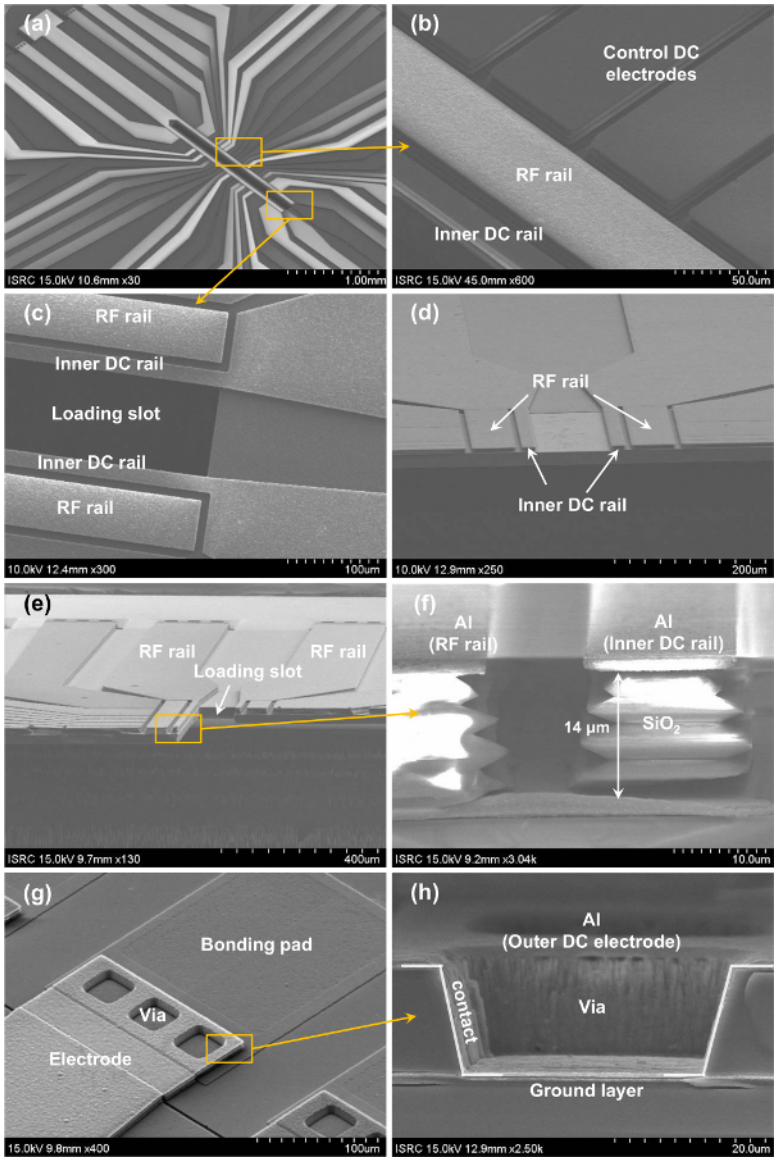

Figure 7: Fabrication results of the surface ion trap. (**a**) Overview of the chip layout. (**b**) A magnified view of the chip layout, which shows the multiple outer DC electrodes. (**c**) A magnified view of chip layout, which shows the loading slot. (**d**) A cross-sectional view of the trapping region before penetrating the loading slot. (**e**) A cross-sectional view of the trapping region after penetrating the loading slot. (**f**) A magnified cross-sectional view of the oxide pillar. The oxide pillars have jagged walls, and the lengths of the overhang are not sufficient, which is attributed to the non-uniform etch rate of the SiO_2 at the interfaces between the separately deposited 3.5 µm-thick SiO_2 layers. (**g**) A top view of a wire-bonding pad of a DC electrode. (**h**) A cross-sectional view of a via. Inclined profiles of the oxide pillars allow for the connection of the DC electrode and the ground layer during the deposition of the Al layer on the sidewall of the oxide pillar instead of filling the via holes with an electroplating process. Please click here to view a larger version of this figure.

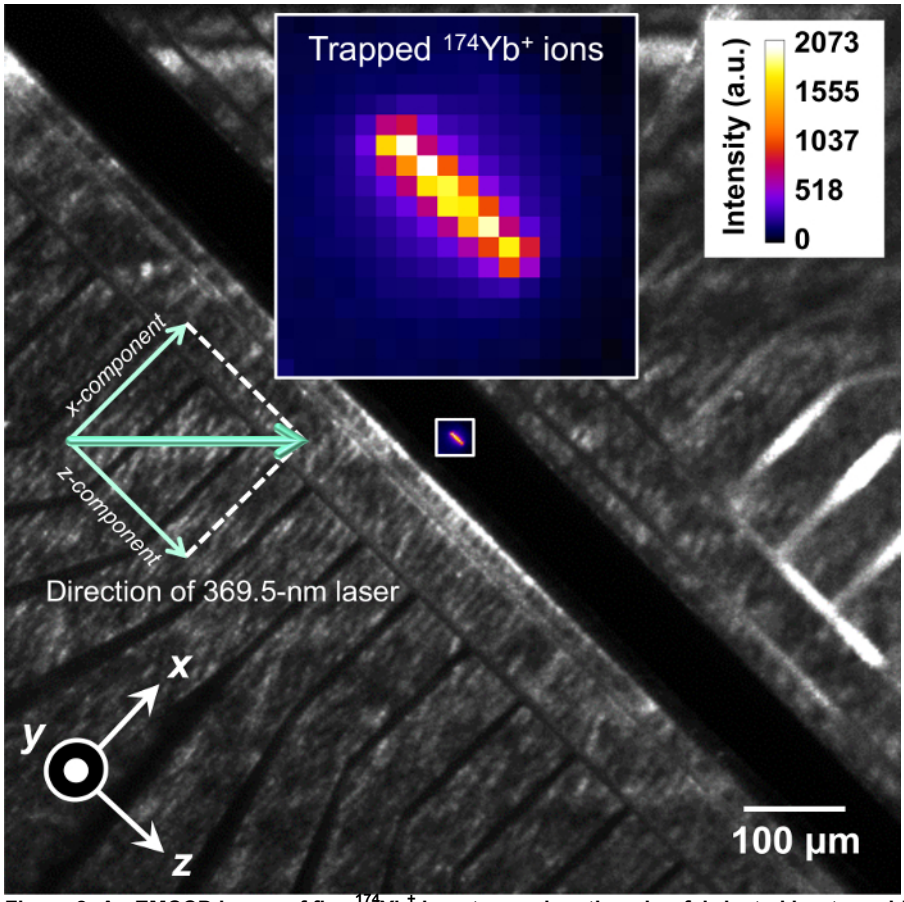

Figure 8: An EMCCD image of five $^{174}Yb^{+}$ ions trapped on the microfabricated ion-trap chip. The image of the surface trap electrode structure was taken separately, and the images of the trapped ion and of the electrodes were combined for clarity. The intensity legend applies only to the pixels in the box. The thick arrow shows the beam path of the 369.5 nm laser and the thin arrows represent the x- and z-components of the momentum of the photon. Please click here to view a larger version of this figure.

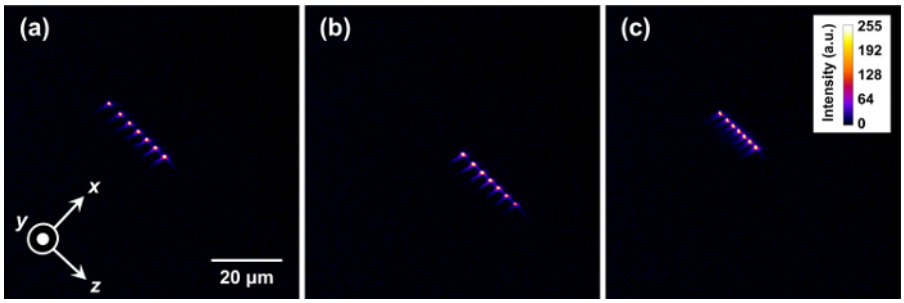

Figure 9: Adjustment of the axial potential of the trapped ions in a linear chain. (**a**) Seven ions at the center of the trap. (**b**) The ions were shuttled tens of micrometers. (**c**) The ion string squeezed in the axial direction. This figure is best viewed as a movie, which is separately uploaded. Please click here to view a larger version of this figure.

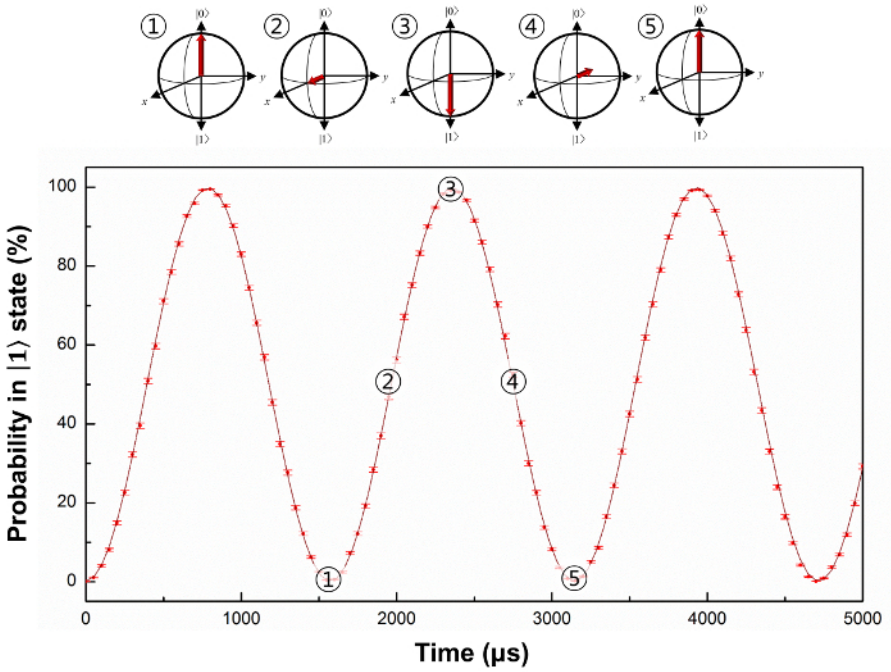

Figure 10: Experimental results of Rabi oscillations between the |0⟩ and |1⟩ states. |0⟩ is defined as the $^2S_{1/2}|F=0, m_F=0\rangle$ state of the $^{171}Yb^+$ ion, and |1⟩ is defined as the $^2S_{1/2}|F=1, m_F=0\rangle$ state. The Rabi oscillation is induced by a 12.6428-GHz microwave. Bloch spheres above the plot show the corresponding quantum states at different times. Please click here to view a larger version of this figure.

Supplementary Document: Please click here to download this document.

Discussion

This paper presented a method for trapping ions using microfabricated surface ion traps. The construction of an ion trapping system requires experiences in various research fields but has not previously been described in detail. This paper provided detailed procedures for microfabricating a trap chip as well as for constructing an experimental setup to trap ions for the first time. This paper also provided detailed procedures for trapping $^{174}Yb^+$ ions and experimenting with trapped ions.

A significant obstacle faced in the microfabrication procedures is the deposition of the dielectric layer, with a thickness of over 10 μm. During the deposition process of the thick dielectric layer, residual stress can build up, which can cause damage to the dielectric film or even break the wafer. To reduce the residual stress, which is generally compressive, a slow deposition rate should be used[40]. In our case, a compressive stress of 110.4 MPa was measured with the deposition conditions of 540 sccm of SiH_4 gas flow rate, 140 W of RF power, and 1.9 Torr of pressure at 5-μm film thickness. However, these process conditions provide only a rough reference, since these conditions can vary significantly for different equipment. In order to reduce the effects of accumulated stress, 3.5 μm-thick SiO_2 films were deposited alternatingly on both sides of the wafer in the presented method. The required thickness of the dielectric layer can be reduced if a smaller RF voltage amplitude and hence a shallower trap depth is chosen. However, a shallower trap depth easily leads to the escape of trapped ions, so the fabrication of thicker dielectric layers, which can withstand higher RF voltages, is more desirable.

There are some limitations to the fabrication method presented in this paper. The lengths of the overhangs are not sufficient to completely hide the dielectric sidewalls from the trapped ions, as shown in **Figure 7f**. Furthermore, the sidewalls of the oxide pillars are jagged, increasing the exposed area of the dielectric sidewalls compared to the vertical oxide pillar. For example, in the case of the sidewall of the inner DC rail near the loading slot with a 5 μm uniform overhang, it is calculated that 33% of the dielectric surface is exposed to the trapped ion position of the vertical sidewall. In the jagged-edge case, more than 70% of the sidewall area is exposed. These non-ideal fabrication results can induce additional stray fields from the exposed dielectrics, but the effects have not been quantitatively measured. Nevertheless, the fabricated chip as reported above has been successfully used in ion trapping and qubit manipulation experiments. In addition, the trap chip presented in this paper has exposed silicon sidewalls near the loading slot. Native oxide can grow on the silicon surfaces and can result in additional stray fields. Therefore, it is recommended to protect the silicon substrate with an additional metal layer, as in[33].

To trap $^{174}Yb^+$ ions, the frequencies of the lasers should be stabilized within a few tens of MHz, and a few different methods are discussed in advanced setups[38,41]. However, for the simple setup discussed in this paper, initial trapping is possible only with stabilization using a wavelength meter.

This paper provided a protocol to trap $^{174}Yb^+$ ions using a microfabricated surface ion-trap chip. Although the protocol for trapping $^{171}Yb^+$ ions is not specifically discussed, the experimental setup described in this paper can be also used to trap $^{171}Yb^+$ ions and to manipulate the qubit state of the $^{171}Yb^+$ ions to obtain Rabi oscillation results (shown in **Figure 10**). This can be done by adding several optical modulators to the output of the lasers and by using a microwave setup, as described in the **Supplementary Document**.

In conclusion, the experimental methods and results presented in this paper can be used to develop various quantum information applications using surface ion traps.

Disclosures

The authors have nothing to disclose.

Acknowledgements

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